REMARKS

Claims 1-4, 6-11, 13 and 14 are all the claims pending in the application. Claim 2 stands rejected on informalities and claims 1-4, 6-11, 13 and 14 stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The 35 U.S.C. §112, Second Paragraph, Rejection

Claim 2 stands rejected under 35 U.S.C. §112, second paragraph. As such, claim 1 has been amended, above, to overcome this rejection. Specifically, proper antecedent basis of "same material" is provided in claim 1 and claim 8.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. The Prior Art Rejections

With respect to the prior art rejections, claims 1-3 and 6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Rostoker (U.S. Patent No. 5,399,898) in view of Zhao et al., hereinafter "Zhao" (U.S. Patent No. 5,674,787) and also as being unpatentable over Kumar et al., hereinafter "Kumar" (U.S. Patent No. 5,290,732) in view of Zhao (U.S. Patent No. 5,674,787). Claims 4 and 7 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Rostoker in view of Zhao and further in view of Chang et al., hereinafter "Chang" (U.S. Patent No.

5,048,744) and Havemann (U.S. Patent No. 6,156,651). Claims 4 and 7 also stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kumar in view of Zhao and further in view of Chang and Havemann. Claims 8-10 and 13 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Rostoker in view of Zhao et al. and also as being unpatentable over Kumar et al. in view of Zhao et al. Claims 11 and 14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Rostoker in view of Zhao et al. and further in view of Chang and Havemann. Claims 11 and 14 also stand rejected under 35 U.S.C. §103(a) as being unpatentable over Kumar in view of Zhao and further in view of Chang and Havemann.

A. The Rejection of Claims 1-3, 6, 8-11 and 13 based on Rostoker in view of Zhao

1. The Position of the Office Action

With respect to claim 1, the Office Action states that Rostoker discloses a metallurgical structure in an integrated circuit (IC)/flip chip having underlying circuitry/components within an exterior covering comprising a passivation/insulating layer (255a in Fig. 2c); a via/hole (260d in Fig. 2c) through the passivation layer extending to a metal line (266b in Fig. 2c); a barrier layer lining the via (262d in Fig. 2c); and a metal plug (264d in Fig. 2c) in the via surrounding the barrier layer wherein the metal plug, barrier layer and the passivation layer form a planar exterior surface of the metallurgical structure; and a solder bump/connector (252d in Fig. 2c) in direct

contact with the conductive/metal plug (264d in Fig. 2c) and the bump being on the planar exterior surface (Fig. 2c; Col. 12, line 14 - Col. 13, line 48; Figs. 1-2c; Cols. 7-13). The Office Action admits, however, that Rostoker fails to specify forming the barrier layer such that the metal plug is above the barrier layer. Nonetheless, the Office Action concludes that Zhao teaches an interconnect structure in an integrated circuit (IC) where a metal/copper plug is above the barrier layer lining (13/16/17 in Fig. 6) the via (Fig.16; Figs.1-14; Col. 5, lines 45- Col, 9, line 10). Therefore, the Office Action concludes that it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a barrier layer lining a via such that the metal plug is above the barrier layer to achieve improved protection/insulation for the interconnect structure using Zhao's barrier protection in Rostoker's structure.

Regarding claim 2, the Office Action asserts that Rostoker fails to specify the metal plug and the line comprising copper. The Office Action contends that Zhao teaches using the metal plug (23 in Fig. 6) and the metal line comprising conventional material such as copper (Col. 5, line 22; Col. 7, line 25). Therefore, the Office Action contends that it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metal plug and the metal line comprising copper to achieve improved electrical performance for the interconnect structure using Zhao's material in Rostoker's structure.

Regarding claim 3, the Office Action suggests that Rostoker discloses a barrier layer lining comprising silicon oxide (262d in Fig. 2c), but the Office Action admits Rostoker fails to specify the barrier layer comprising one or more layers of Ti, TiN, Ta and TaN. The Office Action argues that Zhao discloses the bottom barrier layer comprising TiN, Ta, TaN, etc. Furthermore,

the Office Action concludes that it is conventional in the chip packaging and interconnection technology art to use the materials such as Ti, Cr, Ta, TIN, etc., to improve the resistance against diffusion of impurities and improve adhesion. The Office Action offers that the admitted prior art (APA) specifies using one or more layers of the materials such as Cr, W, Ti, etc., as a barrier layer. Therefore, the Office Action concludes that it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the barrier layer comprising one or more layers of Ti, TiN, Ta and TaN to improve the resistance against diffusion of impurities in Rostoker's structure in view of Zhao. The Office Action states that claim 6 is rejected as explained above for claim 1.

2. The Rostoker Reference

Rostoker discloses that multi-chip, multi-tier semiconductor arrangements based upon single and double-sided flip-chips are described. The double-sided flip chips provide raised bump contact means on both major surfaces of a die and provide connections to internal signals within the die, feed through connections between contacts on opposite sides of the die, and jumpered connections between contacts on the same side of the die. Various multi-chip configurations are described. Certain of these flip-chip configurations dramatically increase the ratio of I/O area (periphery) to footprint area, permitting larger numbers of I/O points within a given assembly footprint than would otherwise be possible in a single die configuration.

3. The Zhao Reference

Zhao discloses a method of utilizing electroless copper deposition to selectively form encapsulated copper plugs to connect conductive regions on a semiconductor. A via opening in an inter-level dielectric (ILD) provides a path for connecting two conductive regions separated by the ILD. Once the underlying metal layer is exposed by the via opening, a SiN or SiON dielectric encapsulation layer is formed along the sidewalls of the via. Then, a contact displacement technique is used to form a thin activation layer of copper on a barrier metal, such as TiN, which is present as a covering layer on the underlying metal layer. After the contact displacement of copper on the barrier layer at the bottom of the via, an electroless copper deposition technique is then used to auto-catalytically deposit copper in the via. The electroless copper deposition continues until the via is almost filled, but leaving sufficient room at the top in order to form an upper encapsulation layer. The SiN or SiON sidewalls, the bottom barrier layer and the cap barrier layer function to fully encapsulate the copper plug in the via. The plug is then annealed.

4. Applicants' Response

The invention replaces the conventional liner 13 with a copper plug 24, 34, 36 and barrier 23, 35. This structure produces a number of advantages when compared to the conventional structure. For example, the copper plug/liner of the invention prevents tin diffusion to the underlying copper wiring layer 20. The copper plug consumes any tin which would otherwise

diffuse the underlying copper wiring. The invention is not limited to copper wiring. Instead, the invention is applicable to any material with similar characteristics as long as the plug and the underlying wiring are of the same material. This allows the plug to consume the potential impurities before they reach the underlying wiring layer. The barrier layer acts to stop any tin impurities which are not consumed by the copper. Further, the invention is different than structures which utilize a thin copper layer in that the copper plug provides sufficient thickness to consume large amounts of tin impurities and to form a strong inter-metallic bond with the lead/tin solder ball.

Additionally, the invention produces a structure which is co-planer with the passivation layer 21, which makes the formation of the lead/tin solder ball 25, 37 simpler and less prone to manufacturing defects. Also, the physical strength of the copper plug/liner structure is superior to the conventional liner 13 (because copper makes a very strong bond with tin/lead solder balls) and, therefore, provides superior mechanical bonding strength between the integrated circuit and the solder ball 25, 37.

The claimed invention is directed to a metallurgical structure that includes a passivation layer, a via through the passivation layer extending to a metal line within the metallurgical structure, a barrier layer lining the via, a metal plug in the via above the barrier layer, the metal plug and the metal line comprising a same material, and a solder bump formed on the metal plug.

The "same material" can be copper and the barrier layer can be one or more layers of Ti, TiN, Ta, and TaN. The barrier layer and the metal plug prevent elements within the solder bump from diffusing to the metal line. Morever, the claimed invention provides for having the metal

plug, the barrier layer and the passivation layer forming a planar exterior surface of the metallurgical structure. The solder ball can be in direct contact with the metal plug or the structure can include a second barrier layer above the metal plug and a second metal plug above the second barrier layer, where the second metal plug is in direct contact with the solder ball.

This formation of a planar exterior surface is not disclosed anywhere in Rostoker. In fact, Rostoker discloses merely a planar exterior surface of the metal plug (264d in Fig. 2c) and the barrier layer (262d in Fig. 2c). The passivation layer (255a in Fig. 2c) is not planar with the metal plug and barrier layer on the exterior surface (254a in Fig. 2c). This important element, in addition to the other features taught, makes the amended claimed invention patentably distinct from the cited prior art. In fact, because the claimed invention produces a structure which is co-planer with the passivation layer 21, it makes the formation of the lead/tin solder ball 25, 37 simpler and less prone to manufacturing defects, a weakness inherent in the cited prior art.

Furthermore, the cited prior art is simply bereft of any language pertaining to the material qualities of the metal plug 24 (264d in Fig. 2c of Rostoker) and the metal line 20 (internal conductor 266b in Fig. 2c of Rostoker). Thus, Rostoker does not teach or suggest having "said metal plug and said metal line comprise a same material." By teaching that the plug and the underlying wiring are of the same material, the claimed invention allows the plug to consume the potential impurities before they reach the underlying wiring layer, which is a quality not realized in the cited prior art.

Therefore, even if Zhao were legally combinable with Rostoker, it would still fail to teach or suggest the structure of the amended claimed invention, namely, that "a metal plug in said via

above said barrier layer, wherein said metal plug and said metal line comprise a same material, and wherein said metal plug, said barrier layer and said passivation layer form a planar exterior surface of said metallurgical structure."

Thus, independent claims 1 and 8 (as well as dependent claims 3, 6, 9-11, and 13) are patentable over Rostoker. Therefore, it is respectfully requested that the Examiner reconsider and remove this prior art rejection.

B. The Rejection of Claims 4, 7, 11 and 14 Based on Rostoker in View of Zhao and Further in View of Chang and Havemann

1. The Position of the Office Action

The Office Action states regarding claim 4 that Rostoker in view of Zhao disclose using the barrier layers to reduce the diffusion of elements and suppress electromigration (Zhao: Col. 5, line 15; Col. 8, lines 7-50) but fail to specify the barrier layer and plug preventing the diffusion of elements within the solder bump into the metal line. However, the Office Action argues that the use of barrier layers such as Ti, TiN, Cr, etc., to provide the diffusion barrier against elements/impurities from solder and to improve adhesion, bond strength and reliability of the interconnection/solder joint, is well-known in the chip packaging and interconnection technology art (see prior art disclosed by Gardner, Col. 1, line 51). The Office Action asserts that

Chang teaches using Cr/Ti barrier layer to improve the diffusion/interaction and enhance conductivity between the solder and the metal such as copper (Col. 7, line 10; Col. 8, line 33; Figs. 8-11). Therefore, the Office Action recites that it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the barrier layer to prevent the diffusion of elements within the solder bump into the metal line and to improve the reliability of the interconnection using Chang's teaching in Zhao's structure in view of Rostoker,

Regarding claim 7, the Office Action argues that Rostoker in view of Zhao fails to specify a second barrier layer above the metal plug and second metal plug above the second barrier layer with the second metal plug being in direct contact with the solder ball. The Office Action further states that Havemann teaches using conventional multilevel structure forming two levels of copper plugs/grooves with TiN barrier layer such that the second barrier layer is above the first metal plug and second metal plug is above the second barrier layer (Fig. 30; Col. 4, line 55- Col. 5, line 38). Therefore, the Office Action concludes that it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a second barrier layer above the metal plug and second metal plug above the second barrier layer with the second metal plug being in direct contact with the solder ball to further prevent the diffusion of elements within the solder bump into the metal line and to improve the reliability of the interconnection using Havemann's teaching in Zhao's structure in view of Rostoker.

2. The Chang Reference

Chang discloses the fluxless bonding in a reducing atmosphere of integrated circuit contacts containing copper is enhanced using a layer of 200 to 1500 Angstrom thick palladium which inhibits copper oxide formation before fusion and reduces all oxides to promote wetting during fusion.

3. The Havemann Reference

Havemann discloses a method of forming mechanically robust vias and entrenched conductors on a dielectric layer (which dielectric layer is on an electronic microcircuit substrate which vias and entrenched conductors are electrically connected to a conductive area on the surface of the substrate) and a structure formed thereby. Generally, some of the dielectric layers added above the microcircuit comprise a porous dielectric having a desirable low dielectric constant but low mechanical robustness. Special methods are described which generally comprise forming the dielectric layer over the substrate; forming a nanaporous dielectric layer over the substrate; depositing a planarizing stopping material over the top surface of said nanaporous dielectric; depositing and patterning photoresist; etching said stopping material and nanaporous dielectric layer in a conductor pattern to expose at least a portion of said conductive area on the surface of said substrate; depositing a wall seal; depositing conductor metal; and planarizing said structure. Generally, the via metal and the conductor metal consist essentially of aluminum,

copper or combinations thereof. The conductor metal may be doped with the selectively deposited via metal being doped by dopant diffusion from the conductor metal, thereby avoiding the difficulty of depositing a doped selective metal. Methods are shown for realizing desirable insulating and conducting layers without deleterious mechanical effects.

4. Applicants' Response

Chang does not disclose a barrier layer and plug that form a planar surface upon which the solder ball can connect. The only drawing in Chang which illustrate a via making contact with a lower metalization layer is Figure 11, and that figure clearly shows a non-planar surface between the solder ball and the underlying layers.

Havemann is referred to as teaching copper plug/grooves within a barrier layer and is not referred to as teaching the claimed planar surface. Indeed, Havemann does not teach or suggest the claimed structure which provides a planar surface upon which to mount the solder ball.

As previously mentioned, the independent claims are patentably distinct over the cited prior art because the prior art fails to teach or suggest the essential elements of the present invention. As such, for the reasons given above, the dependent claims 4, 7, 11 and 14 are patentable, not only by virtue of their dependency from a patentable independent claim, namely, amended independent claims 1 and 8, respectively, but also by virtue of the additional features of the invention that they define. Thus, Applicants respectfully request that this rejection be reconsidered and withdrawn.

C. The Rejection of Claims 1-3, 6, 8-11 and 13 Based on Kumar in view of Zhao

1. The Position of the Office Action

Regarding claim 1, the Office Action states that Kumar discloses a metallurgical structure in an integrated circuit (IC) chip having underlying circuitry/components within an exterior covering comprising a passivation/insulating layer (16b in Fig. 10); a via/hole (Fig. 10) through the passivation layer extending to a metal pad/line (14b in Fig. 9), a barrier layer lining the via (18b in Fig. 10), and a metal plug (40b in Fig. 10) in the via above the barrier layer wherein the metal plug, barrier layer and the passivation layer form a planar exterior surface of the metallurgical structure, and solder bump/connector (44 in Fig. 10) in direct contact with the conductive/metal plug (40b in Fig. 10) and the bump being on the planar exterior surface (Fig. 10; Col. 5, lines 23- Col. 6, line 15; Figs. 5-10; Cols. 3-12).

Regarding claim 2, the Office Action notes, however, that Kumar fails to specify the metal plug and the line/pad comprising copper. The Office Action argues that Zhao teaches using the metal plug (23 in Fig. 6) and the metal line comprising conventional material such as copper (Col. 5, line 22; Col. 7, line 25). Therefore, the Office Action renders that it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the metal plug and the metal line comprising copper to achieve improved electrical performance for the interconnect structure using Zhao's material in Kumar's structure.

Regarding claim 3, the Office Action argues that Kumar discloses a barrier layer lining comprising one or more layers of Ti, TN, Ta and TaN (Col. 3, lines 30 - Col. 4, line 11) to provide the diffusion barrier between the bumps and the metal pad/line. Claim 6 is rejected as explained above for claim 1.

2. The Kumar Reference

Kumar discloses an ionized metal cluster beam deposition of metal bumps on substrates such as multi-chip modules and integrated circuit chips is enhanced. The present invention discloses wet etching techniques for removing unwanted metal deposited on the substrate around bumps, and multiple sources for depositing alloyed (tin-lead) bumps with constant composition.

3. Applicants' Response

As mentioned, the claimed invention, as amended, is directed to a metallurgical structure that includes a passivation layer, a via through the passivation layer extending to a metal line within the metallurgical structure, a barrier layer lining the via, a metal plug in the via above the barrier layer, the metal plug and the metal line comprising a same material, and a solder bump formed on the metal plug.

The "same material" can be copper and the barrier layer can be one or more layers of Ti, TiN, Ta, and TaN. The barrier layer and the metal plug prevent elements within the solder bump

from diffusing to the metal line. Morever, the amended claimed invention provides for having the metal plug, the barrier layer and the passivation layer forming a planar exterior surface of the metallurgical structure. The solder ball can be in direct contact with the metal plug or the structure can include a second barrier layer above the metal plug and a second metal plug above the second barrier layer, where the second metal plug is in direct contact with the solder ball.

Kumar does not contain any language indicating that the metallic bump 40 (Fig. 9) and the chip metal pad 14a (Fig. 9) comprise the same material. In fact, Kumar actually teaches the opposite. Throughout the disclosure of Kumar, chip metal pad 14 is consistently referred to as an "aluminum" pad (see repeated labeling of "aluminum pad" in column 3, for example). Whereas column 5 indicates that the preferred material for the metallic bump 40 is gold. These materials are not the same and, as such, their material qualities are inherently different. This is contrary to the amended claimed invention where the metal plug 24 and the metal line 20 comprise "a same material."

Thus, Kumar does not teach or suggest having "said metal plug and said metal line comprise a same material." By teaching that the plug and the underlying wiring are of the same material, the amended claimed invention allows the plug to consume the potential impurities before they reach the underlying wiring layer, which is a quality not realized in Kumar or any of the other cited prior art.

Therefore, even if Zhao were legally combinable with Kumar, it would still fail to teach or suggest the structure of the amended claimed invention, namely, that "a metal plug in said via above said barrier layer, wherein said metal plug and said metal line comprise a same material, and

wherein said metal plug, said barrier layer and said passivation layer form a planar exterior surface of said metallurgical structure."

Thus, independent claims 1 and 8 (as well as dependent claims 3, 6, 9-11, and 13) are patentable over Kumar. Therefore, it is respectfully requested that the Examiner reconsider and remove this prior art rejection.

D. The Rejection of Claims 4, 7, 11, and 14 Based on Kumar in view of Zhao and further in View of Chang and Havemann

1. The Position of the Office Action

Regarding claim 4, the Office Action states as explained above for claim 1, that Kumar discloses using the barrier layers to reduce the diffusion of elements but fails to specify the barrier layer and plug preventing the diffusion of elements within the solder bump into the metal line. However, the Office Action recites that the use of barrier layers such as Ti, TiN, Cr, etc., to provide the diffusion barrier against elements/impurities from solder and to improve adhesion, bond strength and reliability of the interconnection/solder joint is well-known in the chip packaging and interconnection technology art (see prior art disclosed by Gardner, Col. 1, line 51). The Office Action declares that Chang teaches using Cr/Ti barrier layer to improve the diffusion/interaction and enhance conductivity between the solder and the metal such as copper (Col. 7, line 10; Col. 8, line 33; Figs.8-11). Therefore, the Office Action concludes that it would

have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the barrier layer to prevent the diffusion of elements within the solder bump into the metal line and to improve the reliability of the interconnection using Chang's teaching in Kumar's structure.

With regard to claim 7, the Office Action notes, however, that Kumar fails to specify a second barrier layer above the metal plug and second metal plug above the second barrier layer with the second metal plug being in direct contact with the solder ball. The Office Action argues that Havemann teaches using a conventional multilevel structure forming two levels of copper plugs/grooves with TiN barrier layer such that the second barrier layer is above the first metal plug and second metal plug is above the second barrier layer (Fig. 3G; Col. 4, line 55- Col. 5, line 38). Therefore, the Office Action concludes that it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a second barrier layer above the metal plug and second metal plug above the second barrier layer with the second metal plug being in direct contact with the solder ball to further prevent the diffusion of elements within the solder bump into the metal line and to improve the reliability of the interconnection using Havemann' s teaching in Kumar's structure.

2. Applicants' Response

As previously mentioned, the amended claims are patentably distinct over the cited prior art because the prior art fails to teach or suggest the essential elements of the present invention.

As such, for the reasons given above, the dependent claims 4, 7, 11 and 14 are patentable, not only by virtue of their dependency from a patentable independent claim, namely, amended independent claims 1 and 8, respectively, but also by virtue of the additional features of the invention that they define. Thus, Applicants respectfully request that this rejection be reconsidered and withdrawn.

Insofar as references may be combined to teach a particular invention, and the multiple proposed combinations of Rostoker and Zhao; Rostoker, Zhao, Chang, and Havemann; Kumar and Zhao; and Kumar, Zhao, Chang, and Havemann, case law establishes that before any prior art references may be validly combined for use in a prior-art 35 U.S.C. § 103(a) rejection, the individual references themselves or corresponding prior art must suggest that they be combined.

For example, in In re Sernaker, 217 U.S.P.Q. 1, 6 (C.A.F.C. 1983), the court stated: "[P]rior art references in combination do not make an invention obvious unless something in the prior art references would suggest the advantage to be derived from combining their teachings." Furthermore, the court in Uniroyal, Inc. v. Rudkin-Wiley Corp., 5 U.S.P.Q.2d 1434 (C.A.F.C. 1988), stated, "[w]here prior-art references require selective combination by the court to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gleaned from the invention itself. . . . Something in the prior art must suggest the desirability and thus the obviousness of making the combination."

In the present application, the reason given to support the proposed combination is improper, and is not sufficient to selectively and gratuitously substitute parts of one reference for a part of another reference in order to try to meet, but failing nonetheless, the Applicants' novel

claimed invention. Furthermore, the amended claimed invention meets the above-cited tests for obviousness by including embodiments such as "a metal plug in said via above said barrier layer, wherein said metal plug and said metal line comprise a same material, and wherein said metal plug, said barrier layer and said passivation layer form a planar exterior surface of said metallurgical structure." As such, all of the claims of this application are therefore clearly in condition for allowance, and it is respectfully requested that the Examiner pass these claims to allowance and issue.

As declared by the Federal Circuit:

> In proceedings before the U.S. Patent and Trademark Office, the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992) citing In re Fine, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988).

Here, the Examiner has not met the burden of establishing a prima facie case of obviousness. It is clear that, not only do Rostoker and Kumar fail to disclose all of the elements of the claims of the present invention, particularly the metal plug and the metal line comprising a same material, and the metal plug, the barrier layer and the passivation layer forming a planar exterior surface of the metallurgical structure, as discussed above, but also, if combined with Zhao, Chang, and Havemann, fail to disclose these elements. The unique method of the present invention is clearly an advance over the prior art.

The Federal Circuit also went on to state:

> The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. . . Here the Examiner relied upon hindsight to arrive at the determination of obviousness. It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. Fritch at 1784-85, citing In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

Here, there is no suggestion that either Rostoker or Kumar, alone or in combination with Zhao, Chang, and Havemann, teaches a structure containing all of the limitations of the amended claimed invention. Consequently, there is absent the "suggestion," or "objective teaching" that would have to be made before there could be established the legally requisite "prima facie case of obviousness."

In view of the foregoing, Applicants respectfully submit that Rostoker, Kumar, Zhao, Chang, and Havemann do not teach or suggest the features defined by amended independent claims 1 and 8, and as such, claims 1 and 8 are patentable over Rostoker, Kumar, Zhao, Chang, and Havemann. Further, dependent claims 2 - 4, 6-7, 9-11, and 13-14 are similarly patentable over Rostoker, Kumar, Zhao, Chang, and Havemann, not only by virtue of their dependency from a patentable independent claim, respectively, but also by virtue of the additional features of the invention they define. Thus, Applicants respectfully request that this rejection be reconsidered and withdrawn.

Therefore, it is respectfully requested by Applicants that the Examiner remove the prior art rejections, and pass the application to issue.

III. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-4, 6-11, 13 and 14, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any over payments to Attorney's deposit account number 09-0456.

Respectfully submitted,

Mohammad S. Rahman
Reg. No. 43,029

Dated: 10/16/2001

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Marked Up Version of Changes Made:

IN THE CLAIMS:

Please substitute the following claims for the same numbered claims in the application:

1. (Twice Amended) A metallurgical structure comprising:

a passivation layer;

a via through said passivation layer extending to a metal line within said metallurgical structure;

a barrier layer lining said via;

a metal plug in said via above said barrier layer, wherein said metal plug and said metal line comprise a same material, and wherein said metal plug, said barrier layer and said passivation layer form a planar exterior surface of said metallurgical structure; and

a solder bump formed on said planar exterior surface.

8. (Twice Amended) An integrated circuit structure comprising:

internal components within an exterior covering;

a via extending through said exterior covering to said internal components;

a barrier layer lining said via;

a plug in said via above said barrier layer, wherein said plug and said internal components comprise a same material, and wherein said plug and said barrier layer form a planar exterior surface of said integrated circuit structure; and

a connector formed on said planar exterior surface.